[**Skip to Main Content**](https://www.coursera.org/learn/intro-fpga-design-embedded-systems/exam/WwB1m/mission-002-week-1-quiz/attempt?redirectToCover=true#main)

Top of Form

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* Ubaid Rehman

1. [Introduction to FPGA Design for Embedded Systems](https://www.coursera.org/learn/intro-fpga-design-embedded-systems/home/welcome)
2. [Week 1](https://www.coursera.org/learn/intro-fpga-design-embedded-systems/home/week/1)
3. Mission 002: Week 1 Quiz

[**Previous**](https://www.coursera.org/learn/intro-fpga-design-embedded-systems/peer/VSCEC/mission-001-week-1-application-assignment)[**Next**](https://www.coursera.org/learn/intro-fpga-design-embedded-systems/supplement/b9oKi/week-2-assignment-instructions-and-files)

* **Introduction to the Course**
* **Introduction to the Module**
* **FPGA Origins and Architecture**
* **Logic Design with FPGAs**
* **Week 1 Missions**

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[. Duration: 10 minutes10 min](https://www.coursera.org/learn/intro-fpga-design-embedded-systems/supplement/b9oKi/week-2-assignment-instructions-and-files)

Mission 002: Week 1 Quiz

Quiz30 minutes • 30 min

Review Learning Objectives

**Submit your assignment**

**Due** December 26, 12:59 PM PKTDec 26, 12:59 PM PKT

**Attempts** 1 every 72 hours

Try again

Retake the quiz in **72h**

**Receive grade**

**To Pass** 70% or higher

**Your grade**

60.29%

View Feedback

We keep your highest score

Like

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**Mission 002: Week 1 Quiz**

Graded Quiz. • 30 min

**Due**Dec 26, 12:59 PM PKT

**Try again once you are ready**

**Grade received** 60.29%

**Latest Submission Grade** 60.29%

**To pass** 70% or higher

Retake the assignment in **72h**

**1.**

Question 1

What was missing in CPLDs that created a need for devices like FPGAs ?

**1 / 1 point**



Designs that required many flip-flops



Designs that contained large amounts of sequential circuits



All of the above

**Correct**

Completely correct.

**2.**

Question 2

Which of the following characterize CPLDs ? (**Select all that apply**)

**0 / 1 point**



LUTs

**This should not be selected**

Use of LUTs for logic characterizes FPGAs, not CPLDs



Scales easily to larger devices

**This should not be selected**

Scaling is easier in FPGAs than CPLDs



Predictable



Rich with FFs/registers

**This should not be selected**

FPGAs have higher density of registers than CPLDS.



Easy to design with



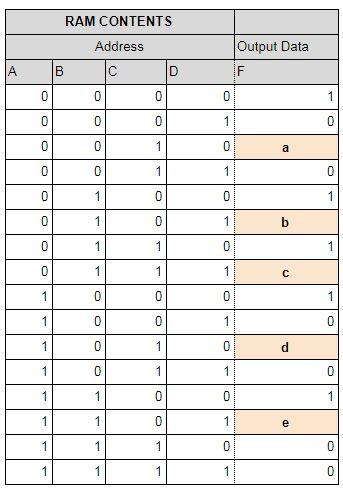
Deterministic

**3.**

Question 3

Fill in the table so that the LUT implements:

**F = (~A & B) | (~C & ~D)**



a = \_\_

b = \_\_

c = \_\_

d = \_\_

e = \_\_

Enter your numerical answers separated by a comma

(example:***x,x,x,x,x*** or **1,1,1,1,1**)

**0 / 1 point**

1,0,0,1,0

**Incorrect**

If you missed this, you might want to review Video 5. Be sure to plugin the values of the inputs in the row to the boolean equation to determine F.

**4.**

Question 4

Which of the following characteristics best match an **ASIC** and which of the following match an **ASSP** device?

**1 / 1 point**



***ASIC***: is a semiconductor device integrated circuit (IC) product that is dedicated to a specific company

***ASSP***: PLD with a fixed OR plane and a programmable AND plane



***ASIC***: is a semiconductor device integrated circuit (IC) product that is dedicated to a specific company

***ASSP***: Is a semiconductor device integrated circuit (IC) product that is dedicated to a specific application market and sold to more than one user



***ASIC***: PLDs that are an integrated circuit designed to be configured by the designer after manufacturing and made up of memory elements (LUTs)

***ASSP***: Is a semiconductor device integrated circuit (IC) product that is dedicated to a specific application market and sold to more than one user



***ASIC***: PLD with a fixed AND plane and a programmable OR plane

***ASSP***: Is a semiconductor device integrated circuit (IC) product that is dedicated to a specific application market and sold to more than one user

**Correct**

Correct for both.

**5.**

Question 5

Which of the following characteristics best matches **PROM** and which of the following best match a **PAL** ?

**1 / 1 point**



***PAL :***PLD with a fixed AND plane and a programmable OR plane

***PROM :***is a semiconductor device integrated circuit (IC) product that is dedicated to a specific application market and sold to more than one user



***PAL :***PLD with a fixed OR plane and a programmable AND plane

***PROM :***PLDs with multiple PALs in the same package with registered outputs and an interconnecting programmable fabric



***PAL :***PLD with a fixed AND plane and a programmable OR plane

***PROM :***PLD with a fixed OR plane and a programmable AND plane



***PAL :***PLD with a fixed OR plane and a programmable AND plane

***PROM :***PLD with a fixed AND plane and a programmable OR plane

**Correct**

Correct for both!

**6.**

Question 6

Which of the following is the best definition for a **CPLD ?**

**0 / 1 point**



A device with multiple PALs in same package with registered outputs and interconnecting programmable fabric



A device with a combination of fully re-programmable AND/OR array and a bank of macrocells that perform combinational and sequential logic



An array of programmable logic blocks, and a hierarchy of reconfigurable interconnects that allow the blocks to be "wired together", like many logic gates that can be inter-wired in different configurations

**Incorrect**

You didn’t select an answer.

**7.**

Question 7

Which of the following characteristics are associated with **SRAM FPGAs** ?

(**Select all that apply** )

**1 / 1 point**



High Reliability



Highest Density

**Correct**

Correct, SRAM FPGAs have the highest logic density due to process advantages.



Reprogrammable

**Correct**

Correct, SRAM FPGAs are reprogrammable.



Expensive



One time Programmable (OTP)



Lowest Cost

**Correct**

Correct, SRAM FPGAs have lower cost due to the process advantages and higher logic density.

**8.**

Question 8

How many**4-input LUTs** with single outputs will be required to implement a **2-bit full adder**with carry?

**0 / 1 point**



2



4



1



3

**Incorrect**

1 LUT only has 4 inputs, you need 5 with carry, so more LUTs are needed

**9.**

Question 9

Does the usage of LUTS for implementation of adders with respect to gates improve delay or performance? Select all that apply..

**1 / 1 point**



decreases delay

**Correct**

True, as the number of gate delays will be larger than the number of LUT delays. The result of the implementation of the 4-bit ripple-carry adder in the Altera MAX10 FPGA is made of a cascade of 4 pairs of 3-input LUTs. The delay through this circuit will be only 4 LUT delays, not 11 gate delays as based on the delay equation of Carry Look ahead adder.



increases delay



increases performance

**Correct**

This is also correct



decreases performance

**10.**

Question 10

Which of the characteristics describe the implementation of a multiplier in an FPGA using Hard Multipliers versus implementation in Memories ? (**Mark all that apply**)

**1 / 1 point**



**Hard Multipliers**: Fast

**Correct**

Correct, Hard multipliers are optimized for speed.



**Hard Multipliers**: Slow



**Memories**: Do not scale easily , Lookup Tables

**Correct**

Correct. Multipliers built of memory do not scale easily as the memory size of the look- up table grows exponentially.



**Memories**: Complex , Lookup Tables

**11.**

Question 11

Which of the characteristics match the implementation of a multiplier in an FPGA using Speciality Circuits, such as the Booth Algorithm ? ( **Mark all that apply )**

**0.75 / 1 point**



Fast

**Correct**

Correct, Booth Algorithm multipliers are fairly fast in execution time



Big



Small

**Correct**

Correct. Booth algorithm multipliers are fairly small in area especially for larger multiplicands



Slow



Complex

**Correct**

Correct. Booth algorithm multipliers are more complex than shifter or memory types



Do not scale easily

**This should not be selected**

Booth algorithm multipliers scale fairly well are numbers get larger



Lookup Tables



State Machine

**12.**

Question 12

Adding FPGA fabric on an SOC makes it a**\_\_\_\_\_\_\_\_\_\_**.

**0 / 1 point**



EPROM



PLA



CPLD



Programmable SoC



Programmable FPGA

**Incorrect**

FPGAs are programmable, but most often not considered a system on a chip.

**13.**

Question 13

What is true for ASICs relative to FPGAs? (Select all that may apply)

**0.5 / 1 point**



Lower speed



High cost per unit

**This should not be selected**

This is incorrect



ASICs have lower cost per unit.



Higher speeds

**Correct**

Correct. ASICs generally have higher speed than FPGAs

**14.**

Question 14

What are the principal advantages of FLASH based FPGAs over SRAM based FPGAs ? (**Mark all that apply**)

**1 / 1 point**



Faster Speed



Lower Power

**Correct**

Correct. FLASH FPGAs have lower leakage and consume much less static power.



Higher Reliability

**Correct**

Correct. FLASH FPGAs are more reliable, with SEU immunity



Better Security

**Correct**

Correct. FLASH FPGAs are a single chip solution that is difficult to reverse engineer once the security fuse is blown.

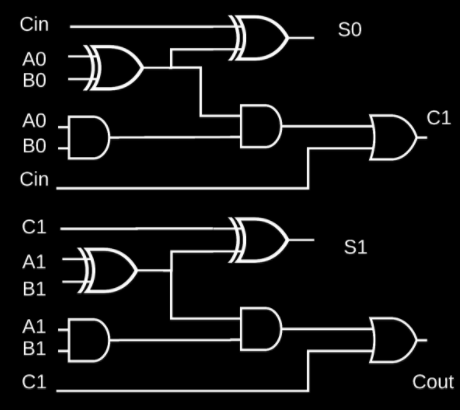
**15.**

Question 15

Which of the following is the best implementation for a 2-bit full adder. Hint: make sure to pay attention to signal names as well as circuit diagram.

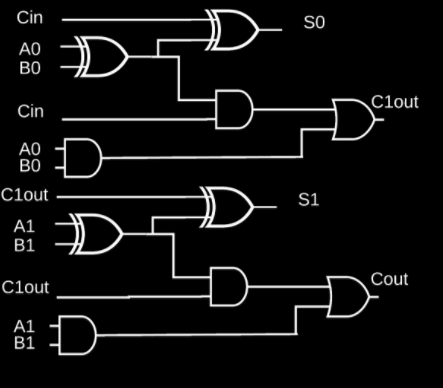
**0 / 1 point**





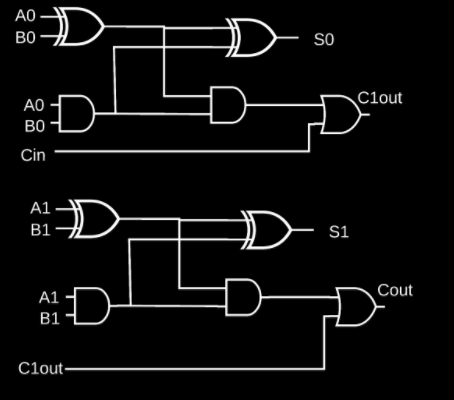
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**Incorrect**

If you missed this, you might want to review Video 6

**16.**

Question 16

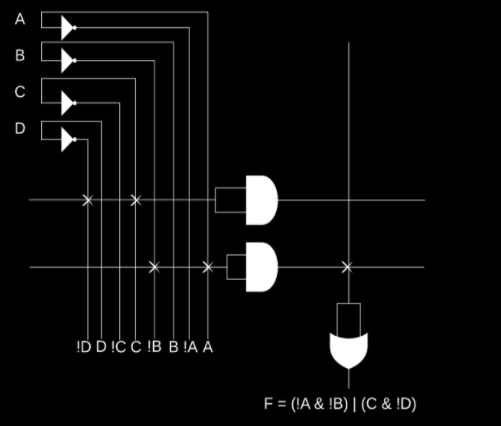
Choose the best implementation of the logic equation

**(NOT(A) AND NOT(B)) OR (C AND NOT(D))**

**using PLA options:**

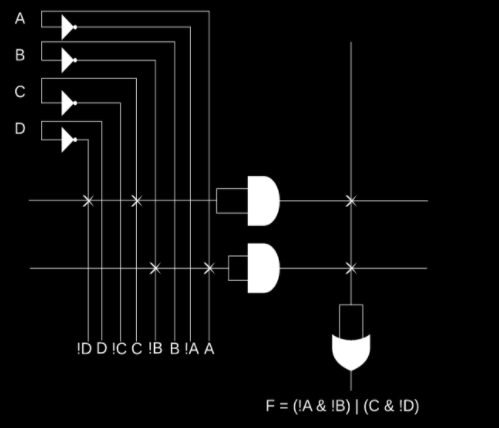
**1 / 1 point**





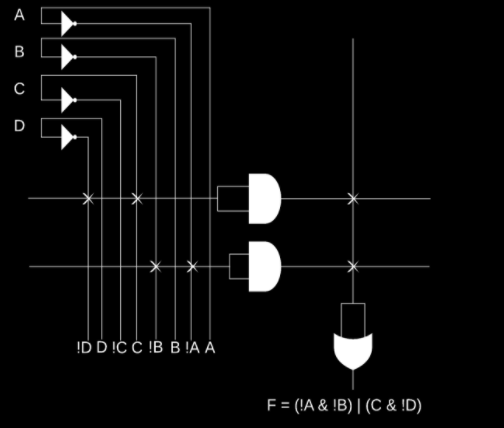
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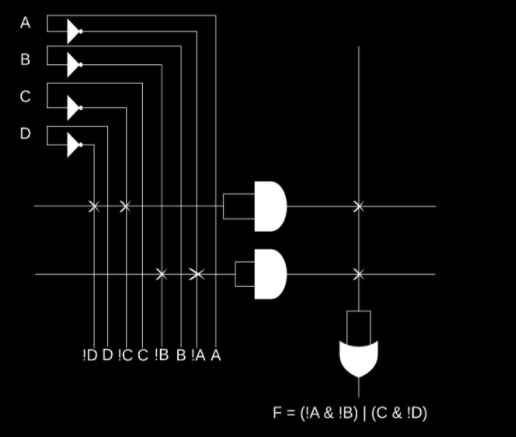
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**Correct**

**17.**

Question 17

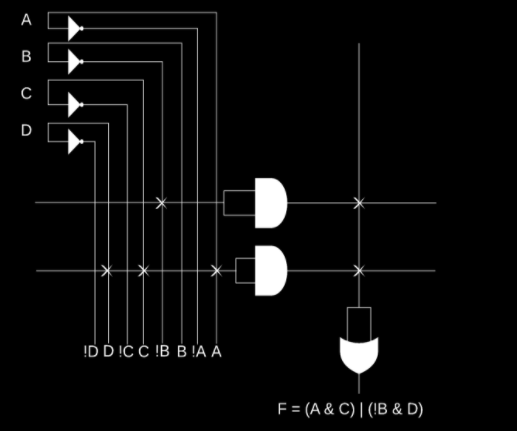
**Choose the correct implementation of logic equation**

**((A) AND (C)) OR (NOT(B) AND D)**

**using PLA options:**

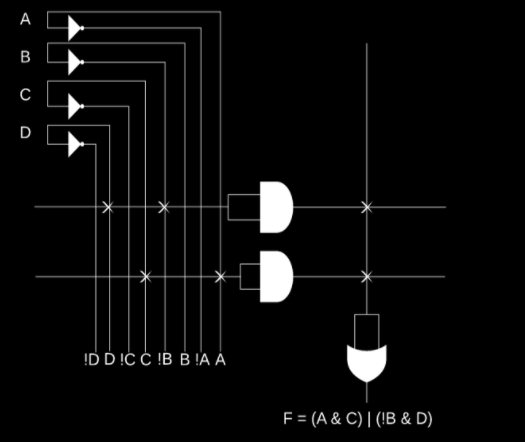
**1 / 1 point**





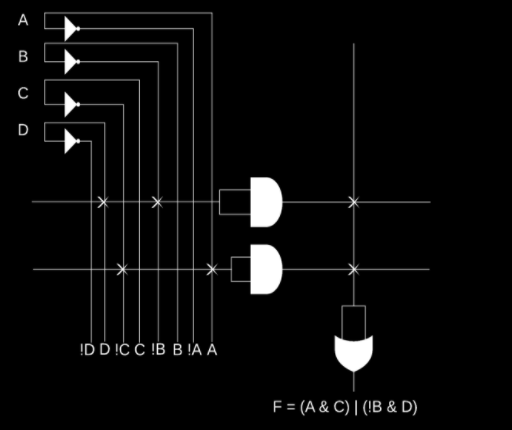
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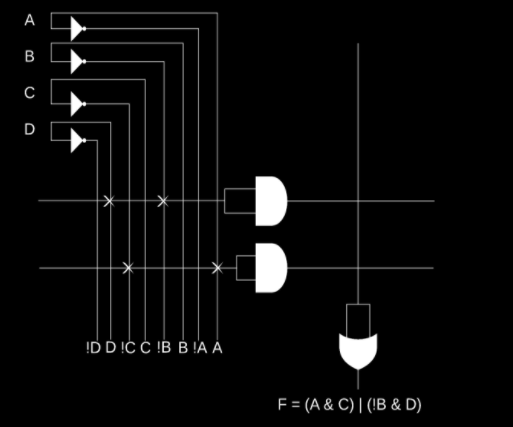
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**Correct**